



# IDT Gen 2 Serial RapidIO™ SERDES IBIS-AMI Model User Manual

Formal Status  
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## About this Document

Topics discussed include the following:

- [Transmitter Model](#)
- [Receiver Model](#)

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## Revision History

September 12, 2011, Formal

Revised to include process corners.

Updated behavioural curves.

June 3, 2011, Formal

Initial release.

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## Introduction

As the speed of serial data links has increased, signal integrity analysis has become more important. Signals have progressed to operating at speeds where the PCB materials and layout topology have a profound effect on the quality of the signal seen at the data receiver. In the past, IBIS V-I curves were sufficient in modelling the data path and its transmitter and receiver components. However, IBIS V-I simulations tend to lose their correlation at operating frequencies greater than 800Mhz. The need for accurate models forced users to h-spice models constructed as behavioural or extracted from the transistor design. Though very accurate, these models tend to have very slow run-times which are insufficient for modelling serial links containing large data sequences. Modelling topologies in an attempt to confirm bit-error-rates of less than  $10^{-12}$  take days of processing time. The advent of IBIS-AMI modelling brought together V-I curves and behavioural models into one package that are capable of processing simulations of one million bits per minute. Incorporating statistical methods into time domain modelling allows prediction of bit-error-rates as low as  $10^{-23}$ .

This IBIS-AMI (AMI) model is provided to customers to permit them to model their topologies incorporating the CPS/VPS1848, CPS/SPS/VPS1616, CPS1432 Gen 2 Serial RapidIO switches. The same model is applicable to all of the devices listed.

The models are composed of three distinct blocks: an analog model, an algorithmic model and tool interpreted block describing the user interface. Combined together they form a complete model. The .ibs portion describes the electrical behaviour of the transmitter or receiver. The .ami portion describes to the simulator the user interface and the ranges of I/O values. Parts of the .ami file are conditionally used based on the capabilities available in the simulator. Simulators that are not able to use that information are expected to ignore it. The .dll is the algorithmic model of the transmitter or receiver and it describes the functional behaviour of the model.

This document discusses the transmitter and receiver model behaviours, exposes the basic architectures and explains the parameters available from the user interface.

## Transmitter Model

The transmitter is a 6.25 Gbps capable RapidIO SerDes device that has controls for three taps. The taps are the pre-emphasis, amplitude and post-emphasis.

### Operation

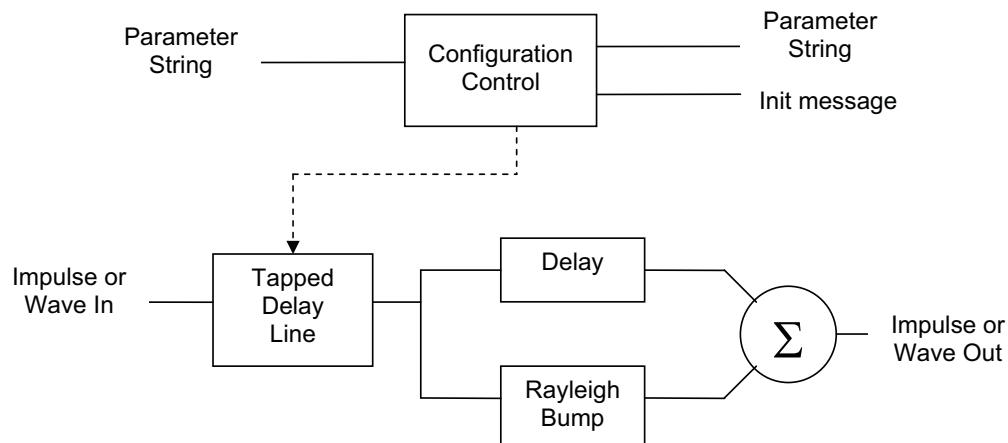
This model has the following features and control settings.

The user inputs/controls to this model will be:

- Amplitude
  - Driver output amplitude
  - AMI Model parameter name: Tx\_Amp\_Ctrl
  - 64 settings
  - Default Setting: 0b100000 (d'32)
  - Suggested settings:
    - The long run range is d'40 (0b101000) to d'63 (0b111111).
    - If 5 Gbps or above, short run nominal is d'28 (0b011100), if below 5 Gbps, the nominal is d'32 (0b100000). The short run range is d'0 to d'39 (0b100111).
- Pre-emphasis
  - Driver pre-emphasis level
  - AMI Model parameter name: Tx\_Pre\_Tap\_Ctrl
  - 32 settings
  - Default Setting: 0
  - Valid settings: d'0 to d'31 (0b11111)
- Post-emphasis
  - Driver post-emphasis level
  - AMI Model parameter name: Tx\_Post\_Tap\_Ctrl
  - 64 settings
  - Default Setting: 0
  - Valid settings: d'0 to d'63 (0b111111)
- PVT variation
  - 3 corners selectable:
    - TT @ 25 deg C
    - SS @ -43 deg C
    - FF @ 95 deg C

## Block Diagram

Figure 1: Transmitter Model Block Diagram



## Model Behaviour

### Analog Model Parameters

The output impedance and capacitance values were generated from the HSPICE model by varying the termination voltage and observing small changes in the step response. The behaviour of the amplitude, pre and post taps was obtained through lab measurements. This resulted in the following four graphs showing the transmit swing, output impedance as a function of Tx\_Amp\_Ctrl, pre and post tap de-emphasis.

The output capacitance is estimated to be 0.95pF per pin.

Figure 2: Differential Output Voltage vs. Tx\_Amp\_Ctrl with TX\_PRE\_TAP\_CTRL=0, TX\_POST\_TAP\_CTRL=0

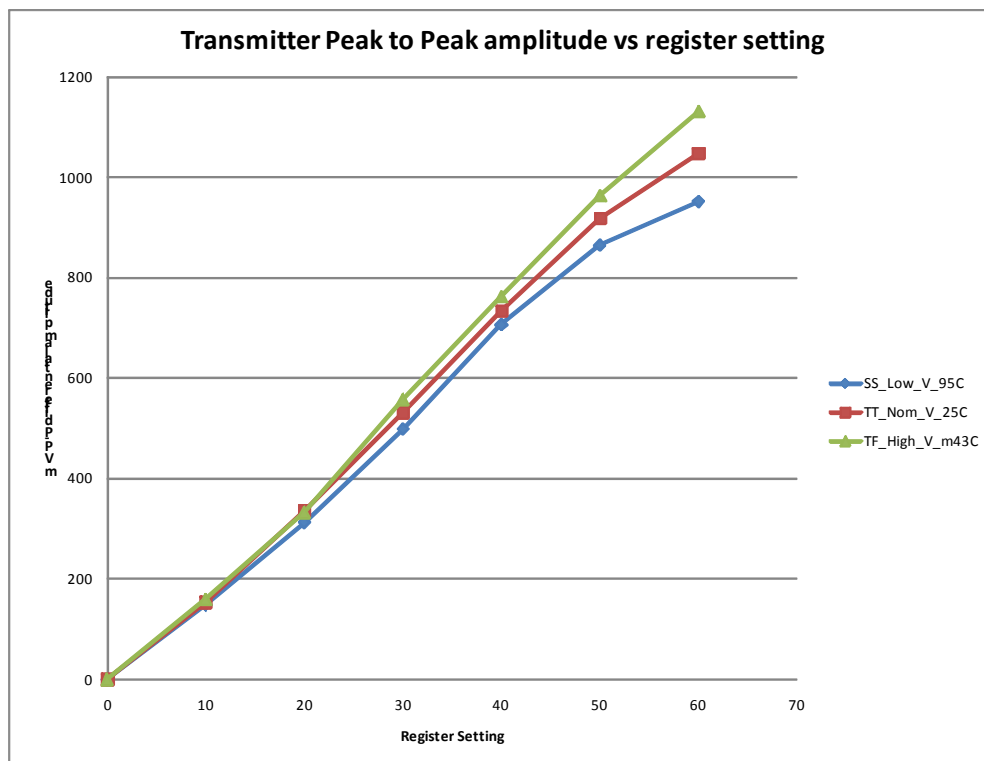


Figure 3: Differential Output Resistance vs. Tx\_Amp\_Ctrl

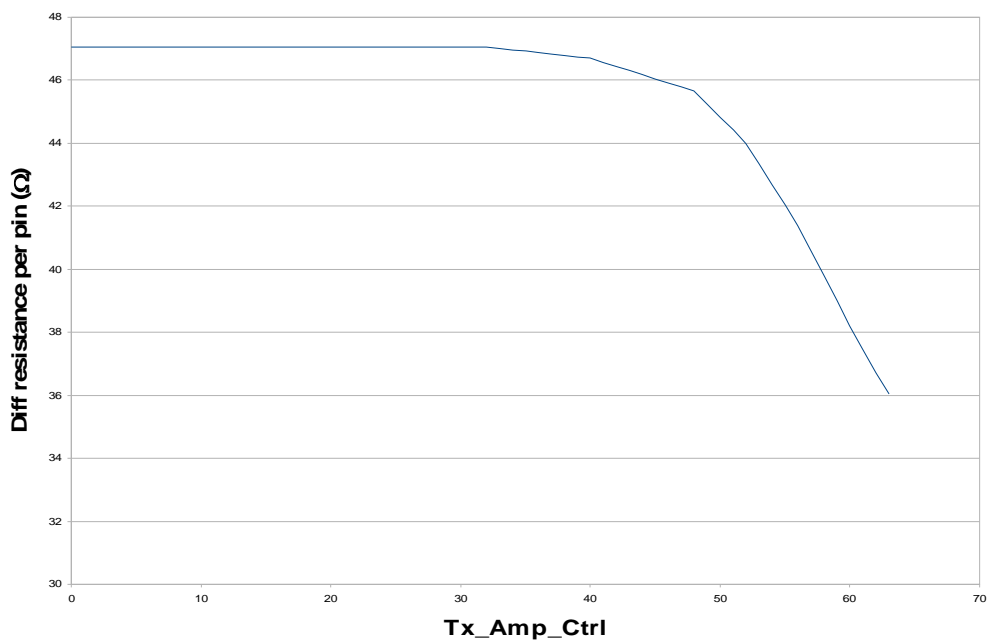


Figure 4: TX\_POST\_TAP\_CTRL behaviour with TX\_AMP\_CTRL=60, PRE\_TAP=0

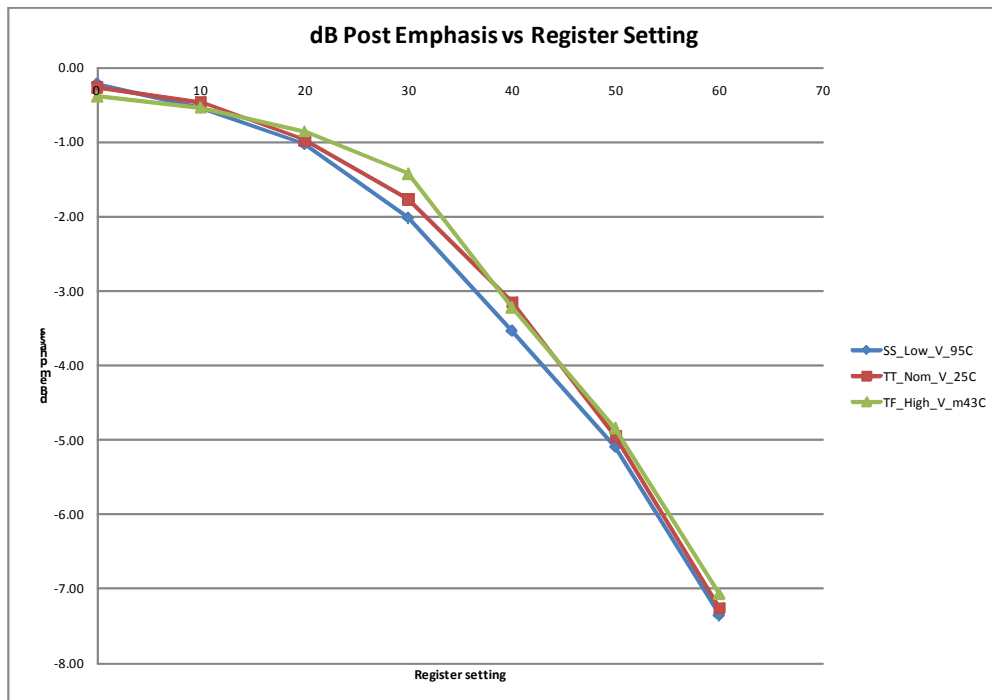
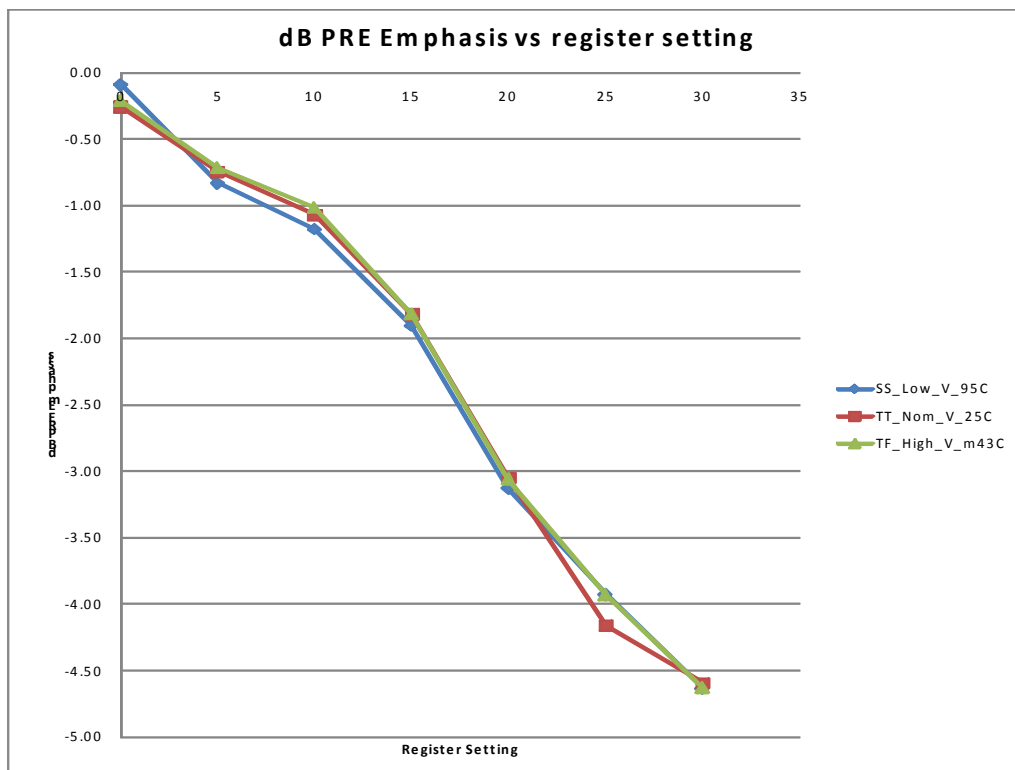


Figure 5: TX\_PRE\_TAP\_CTRL behaviour with TX\_AMP\_CTRL=60, TX\_POST\_TAP\_CTRL=0



## Pre- and Post-emphasis Parameters

The transmit tap weights of Tx\_Amp\_Ctrl, Tx\_Pre\_Tap\_Ctrl, and Tx\_Post\_Tap\_Ctrl, normalized to unity, are:

$$G_{pre} = -0.0081 * Tx\_Pre\_Tap\_Ctrl$$

$$G_{post} = -0.0054 * Tx\_Post\_Tap\_Ctrl$$

$$G_{main} = 1 + G_{pre} + G_{post}$$

## Register Interface

The register interface implementation in the devices accepts the hex equivalent of the decimal value entered into the AMI model.

The TX\_AMP\_CTRL field is located in bits 21-26 of the LANE\_n\_CTRL\_CSR.

The TX\_PRE\_TAP\_CTRL field is located in bits 21-25 of the LANE\_n\_STATUS\_3\_CSR.

The TX\_POST\_TAP\_CTRL field is located in bits 26-31 of the LANE\_n\_STATUS\_3\_CSR.

## Simulation tool usage of IBIS and AMI files

The .IBS and .ami files contain information that describes to a simulator how that I/O cell must behave. In a large number of tools, these files are never viewed by the user because the tool extracts the user parameters and presents them to the user in a friendly fashion.

The complete IBIS-AMI model of a transmitter and receiver pair consists of five files:

- the .ami files which contain the electrical characteristics to allow the simulator to extrapolate information instead of being provided explicit values. The file also contains default values, and ranges of coefficients for checking purposes before passing the values to the dll. One file is required for each the transmitter and receiver.
- the .dll file which is the heart of the model. The .dll contains the algorithmic portion of the simulation model, in contrast to the .ibs which contains the electrical characteristics of the model. One file is required for each the transmitter and receiver.
- the .ibs file which contains the electrical data for the simulator. This file contains electrical models from both the receiver end and the transmitter.

Some tools require that the files be wrapped by an interface layer of code by the user before they can be used. The user must manually parse the files and determine what parameters must be brought out in order to correctly manipulate the model.

The .IBS and .AMI files are text files and are human readable, exposing all of the model parameters to the user, some of which are expressly intended for the simulator to interpret, and not the user. The following Transmitter and Receiver sections below explain the user configurable and selectable parts of the files for tools which require the user to manually extract the "user parameters".

### Transmitter

The .IBS file contains 63 models, one for each TX\_AMP\_CTRL setting available. In order to obtain the correct transmitter drive strength in the simulation the user must specifically choose the desired model and pass its name to the simulator. For example, for a desired drive strength of 23 decimal, the user must pass the model name "idt\_corvette\_ami\_tx\_23" to the simulator. Each model will provide to the simulator the voltage swing, output impedance, rise and fall times. The model will also provide to the simulator the names of the .ami file and the .dll file.

No edits of the .ibs file are to be made by the user.

The .ami file contains three distinct sections:

- Reserved Parameters
- Model Specific
- Advanced Capability

The Reserved Parameters section must not be edited by the user.

In the Model Specific section, only the "Default" value can be changed by the user. Modification of any other fields will result in a simulator error.

In the section beginning with the comment: "Advanced capability as defined by IBIS Birds 118-124", there is no user friendly information present even though the text is descriptive. The content from this comment to the end of the file is expressly provided for the simulator to read and interpret. If a simulator is not compliant to IBIS BIRDS 118-124, the simulator will ignore the informatin in this section and instead extract it from the VI data present in the .ibs file. No information is lost by the lack of capability of the simulator, only speed and efficiency is affected.

## Receiver Model

The receiver consists of a preamplifier, a clock recovery loop and a DFE subsystem that controls input gain and DC offset in addition to DFE tap values.

The receiver can accept coefficients from the user or can be used in an adaptive mode and derive coefficients for the user.

## Operation

The operation of the receiver is controlled by Tap coefficients and option switches provided in the model.

The following option switches are available to users but are required to be left in their default settings when modelling the real silicon:

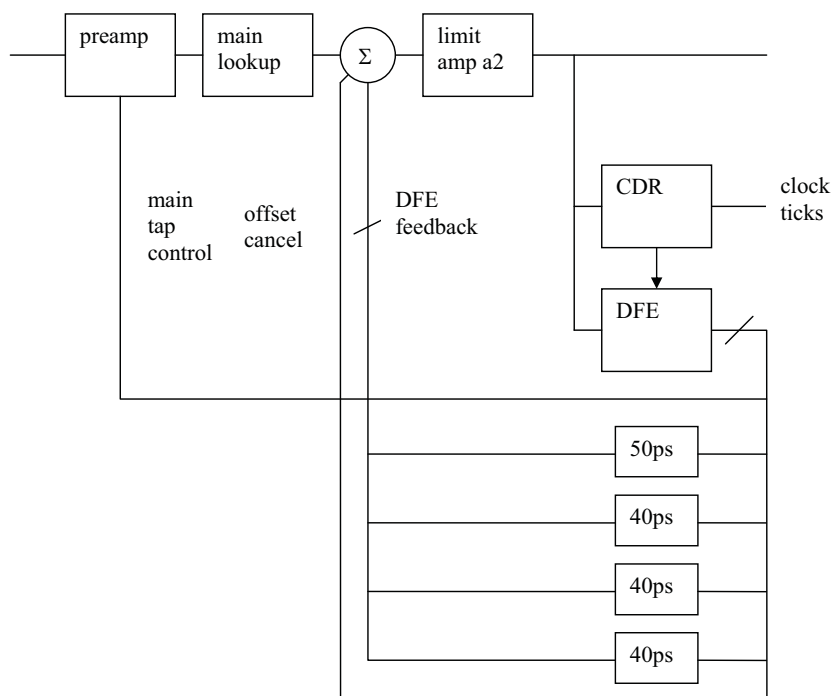
- offset\_cancel
- CDR.mode
- CDR.phase\_out
- CDR\_ref
- coeff.offset\_cancel

The option switches were provided in the model for testing and correlation purposes only.

- PVT variation
  - 3 corners selectable:
    - TT @ 25 deg C
    - SS @ -43 deg C
    - FF @ 95 deg C



Figure 6: Model Block Diagram



## Tap coefficients

In the IBIS-AMI model, the main tap setting (VGA: VariableGainAmplifier control), dfe taps, and offset cancellation are all controlled by an array of six coefficients. Within this array, the individual coefficients are:

- coeff.0: The main tap coefficient (VGA). This user coefficient finds its way to the preamp, where it is used to set the source resistance in the first stage seen by the DFE Tap adders.
- coeff.1: First DFE tap coefficient. This user coefficient affects the ISI at 1UI after the main tap.
- coeff.2: Second DFE tap coefficient. This user coefficient affects the ISI at 2UI after the main tap.
- coeff.3: Third DFE tap coefficient. This user coefficient affects the ISI at 3UI after the main tap.
- coeff.4: Fourth DFE tap coefficient. This user coefficient affects the ISI at 4UI after the main tap.
- coeff.5: DC differential offset cancellation. This user coefficient adjusts the common mode offset of the receiver. Users are not required to adjust this coefficient from the zero default value.

The AMI model coefficients are scaled differently than the silicon implementation in the actual device. Their ranges are compared in [Table 1](#).

Table 1: Coefficient range cross-reference summary.

AMI Model Tap Coefficient Label	Register Tap Coefficient Label	Register Value Range
coeff.0	TAP_0_CONFIG	0 to +15
coeff.1	TAP_1_CONFIG	0 to +31
coeff.2	TAP_2_CONFIG	-15 to +15
coeff.3	TAP_3_CONFIG	-7 to +7
coeff.4	TAP_4_CONFIG	-3 to +3
coeff.5	TAP_OFFSET_CONFIG	-31 to +31

Please refer to the Appendix tables to cross reference the AMI model produced coefficients to register values that can be applied to the SERDES control register in the actual device.

## Manual Coefficient Switch

A switch named "coeff.mode" has been provided in the IBIS-AMI model to allow the coefficients to be set manually. This parameter will control coefficients 1-4 as follows:

- off – Coefficients 1-4 are set to zero and no adaptation will occur in either statistical analysis or time domain simulation.
- fixed – Coefficients 1-4 are set by the input parameter string and will retain these values through both statistical analysis and time domain simulation.
- auto – Near optimal values for coefficients 1-4 are calculated for statistical analysis, and those values are used as the starting values for time domain simulation. During time domain simulation, the DFE loop is fully adaptive.
- adapt – Near optimal values for coefficients 1-4 are calculated for statistical analysis, but then the coefficients are set to zero as the starting values for time domain simulation. During time domain simulation, the DFE loop is fully adaptive.

## VGA\_mode

The IBIS-AMI model provides a separate control for the main tap coefficient, coeff.0. The supported values for this control are

- off – Coefficient 0 is set to its default value of 8.
- fixed – Coefficient 0 is set to a fixed value by the input parameter string.
- auto – Coefficient 0 is set to a near optimal value for statistical analysis, that value is used as the starting value for time domain simulation, and the main tap loop is fully adaptive.
- adapt – Coefficient 0 is set to a near optimal value for statistical analysis, the starting value for time domain simulation is 8, and the main tap loop is fully adaptive.

## offset\_cancel

The IBIS-AMI model provides a switch in order to control the DC offset cancellation loop. The offset affected is common mode caused by unequal bit energy as a result of losses through a long transmission line. A value of 1 enables the loop and the default value of 0 disables the loop. It is not recommended for users to turn off the DC offset cancellation loop.

## CDR1

The IBIS-AMI model provides control of the clock recovery loop labeled CDR1. There is a switch for setting the phase manually. It is not recommended for users to modify any parameters of the CDR1 type. The default values are sufficient for the operation of the model. The available parameters are:

- CDR1.phase\_out: The clock phase, as a number from 0 to 255. This number can be set in the input parameter string, and will also be reported in the output parameter string, for statistical analysis and time domain simulation.
- CDR1.mode: The control mode for the clock recovery loop. The supported values are:
  - off – Clock phase is zero for both statistical analysis and time domain simulation
  - fixed – Clock phase is set by the input parameter string and remains at that value for both statistical analysis and time domain simulation.
  - auto – The near optimum clock phase is calculated for statistical analysis and used as the starting value for time domain simulation. The clock recovery loop is fully adaptive in time domain simulation.
  - adapt – The near optimum clock phase is calculated for statistical analysis; however the starting value for time domain simulation is zero. The clock recovery loop is fully adaptive in time domain simulation.

## CDR1.ref

AMI simulations run fast enough that it is practical to simulate an offset between the transmit and receive reference clocks. IDT is therefore including the reference clock offset, as a fraction of the reference clock frequency, in the parameters for the clock recovery loop. Users may insert an offset of up to 100ppm in this parameter.

# Description

## Model Input Characteristics

The analog model for the receiver consists of  $50\Omega$  and  $0.95\text{pF}$  to virtual ground for both the true and complement pins.

The ESD protection device is included in the receiver model.

## Preamplifier

The preamplifier consists of two amplifier stages. Each stage is described using a nonlinear second order differential equation derived from the design. There are no controls provided for these amplifiers.

## DFE

To ease timing in the DFE feedback path of the silicon, the DFE is organized into an odd/even architecture permitting the silicon to operate at one half of the data rate. The IBIS AMI specification only directly supports a single, albeit virtual data decision point. For this AMI model, therefore, the decision point is a composite of the slicing latches on both the odd and even sides of the circuit. The result is that for each transmitted data bit, the waveform output from the model will be the waveform at the latch which is actually making the data decision for that bit. While this will introduce unrealistic discontinuities at the edges of the eye diagram, these discontinuities will not affect the performance analysis (in the center of the eye).

A limiting amplifier is present between the output of the preamp and the point where the DFE feedback is added into the signal, and a second one between the point where the DFE feedback is added into the signal and the data decision point.

Feedback for the DFE is obtained by detecting the data using sampling latches that are offset by  $\pm V_{ref}$ . This generates an error signal in addition to the data signal. When the signal at the sampling time is outside the voltage range  $\pm V_{ref}$ , then the error signal matches the data. Otherwise, the two signals are opposite each other. For each DFE tap, the tap value is the integral of the current error signal times the data that was driving the DFE tap at the time the error signal was detected. The net result is that the DFE loop works to minimize the difference between the signal at the sampling time and  $\pm V_{ref}$ . The sample threshold is  $\pm 50\text{mV}$ , so signals must have a minimum eye opening of at least  $100\text{mV}$  peak to peak in order to be detectable.

## Clock Recovery

Clock recovery in the model is a classic first order clock recovery loop. There are 256 clock phases in the half rate clock, linearly interpolated. A loop update is made once every twenty bits, with four low speed clock cycles of delay in the feedback loop. Each early or late phase detection is equivalent to one quarter of a phase step, or  $1/1024$  of a UI.

## Register Interface

The register interface implementation in the devices accepts the hex equivalent of the decimal value entered into the AMI model.

The TAP\_OFFSET\_CONFIG field is located in bits 3-8 of the LANE\_n\_DFE\_2\_CSR.

The TAP\_4\_CONFIG field is located in bits 9-11 of the LANE\_n\_DFE\_2\_CSR.

The TAP\_3\_CONFIG field is located in bits 12-15 of the LANE\_n\_DFE\_2\_CSR.

The TAP\_2\_CONFIG field is located in bits 16-20 of the LANE\_n\_DFE\_2\_CSR.

The TAP\_1\_CONFIG field is located in bits 21-26 of the LANE\_n\_DFE\_2\_CSR.

The TAP\_0\_CONFIG field is located in bits 27-30 of the LANE\_n\_DFE\_2\_CSR.

The AMI model tap coefficients must be converted using the following tables before being entered into the register fields.

Table 2: TAP 0 Value Conversion from Model to Device

AMI Model TAP 0 implementation	Device TAP_0_CONFIG register field binary equiv
15	1111
14	1110
13	1101
12	1100
11	1011
10	1010
9	1001

AMI Model TAP 0 implementation	Device TAP_0_CONFIG register field binary equiv
8	1000
7	0111
6	0110
5	0101
4	0100
3	0011
2	0010
1	0001
0	0000

Table 3: TAP 1 Value Conversion from Model to Device

AMI Model TAP 1 implementation	Device TAP_1_CONFIG register field binary equiv
31	011111
30	011110
29	011101
28	011100
27	011011
26	011010
25	011001
24	011000
23	010111
22	010110
21	010101

AMI Model TAP 1 implementation	Device TAP_1_CONFIG register field binary equiv
20	010100
19	010011
18	010010
17	010001
16	010000
15	001111
14	001110
13	001101
12	001100
11	001011
10	001010
9	001001
8	001000
7	000111
6	000110
5	000101
4	000100
3	000011
2	000010
1	000001
0	000000

Table 4: TAP2 Value Conversion from Model to Device

AMI Model TAP 2 implementation	Device TAP_2_CONFIG register field binary equiv
15	11111
14	11110
13	11101
12	11100
11	11011
10	11010
9	11001
8	11000
7	10111
6	10110
5	10101
4	10100
3	10011
2	10010
1	10001
0	10000
-1	01111
-2	01110
-3	01101
-4	01100
-5	01011
-6	01010
-7	01001
-8	01000

AMI Model TAP 2 implementation	Device TAP_2_CONFIG register field binary equiv
-9	00111
-10	00110
-11	00101
-12	00100
-13	00011
-14	00010
-15	00001

Table 5: TAP 3 Value Conversion from Model to Device

AMI Model TAP 3 implementation	DeviceTAP_3_CONFIG register field binary equiv
7	1111
6	1110
5	1101
4	1100
3	1011
2	1010
1	1001
0	1000
-1	0111
-2	0110
-3	0101
-4	0100



AMI Model TAP 3 implementation	DeviceTAP_3_CONFIG register field binary equiv
-5	0011
-6	0010
-7	0001

Table 6: TAP4 Value Conversion from Model to Device

AMI Model TAP 4 implementation	Device TAP_4_CONFIG register field binary equiv
3	111
2	110
1	101
0	100
-1	011
-2	010
-3	001

Table 7: TAP5 Value Conversion from Model to Device

AMI Model TAP 5 implementation	Device TAP_OFFSET_CONFIG register field binary equiv
31	111111
30	111110
29	111101
28	111100
27	111011
26	111010
25	111001
24	111000

AMI Model TAP 5 implementation	Device TAP_OFFSET_CONFIG register field binary equiv
23	110111
22	110110
21	110101
20	110100
19	110011
18	110010
17	110001
16	110000
15	101111
14	101110
13	101101
12	101100
11	101011
10	101010
9	101001
8	101000
7	100111
6	100110
5	100101
4	100100
3	100011
2	100010
1	100001
0	100000

AMI Model TAP 5 implementation	Device TAP_OFFSET_CONFIG register field binary equiv
-1	011111
-2	011110
-3	011101
-4	011100
-5	011011
-6	011010
-7	011001
-8	011000
-9	010111
-10	010110
-11	010101
-12	010100
-13	010011
-14	010010
-15	010001
-16	010000
-17	001111
-18	001110
-19	001101
-20	001100
-21	001011
-22	001010
-23	001001
-24	001000

AMI Model TAP 5 implementation	Device TAP_OFFSET_CONFIG register field binary equiv
-25	000111
-26	000110
-27	000101
-28	000100
-29	000011
-30	000010
-31	000001



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